CS162 Operating Systems and Systems Programming Lecture 3

**Processes (Continued)** 

Professor Natacha Crooks & Matei Zaharia https://cs162.org/

Slides based on prior slide decks from David Culler, Ion Stoica, John Kubiatowicz, Alison Norman and Lorenzo Alvisi

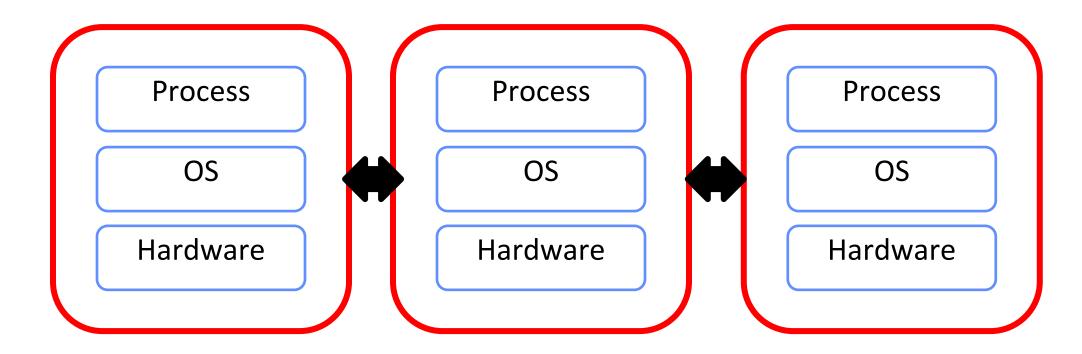
## Drop now (by Jan 31<sup>st</sup>) or forever hold your peace

## (aka stay enrolled in CS162)

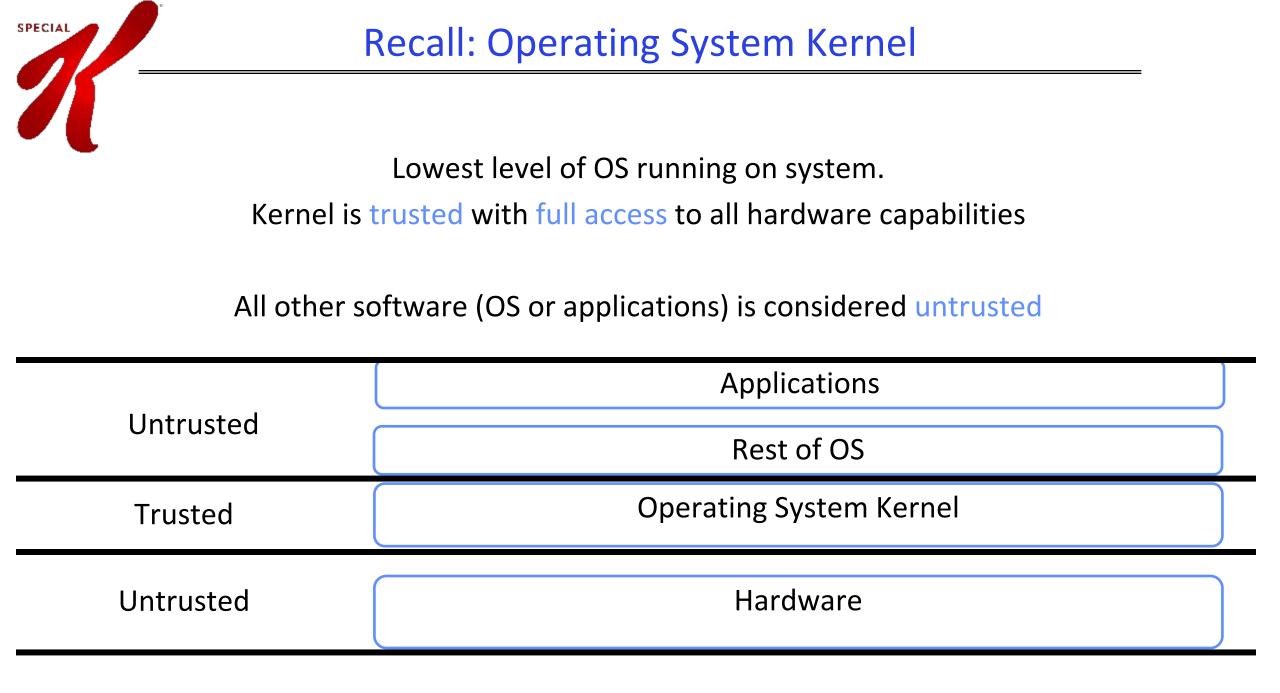
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### **Recall: The Process**

#### A executing program with restricted rights



Enforcing mechanism must not hinder functionality or hurt performance



**Recall: Dual Mode Operation** 

Use a bit to enable two modes of execution

In User Mode

In Kernel Mode



Processor checks each instruction before executing it

Executes a limited (safe) set of instructions

OS executes with protection checks off

Can execute any instructions

### Recall: Hardware must support

#### 1) Privileged Instructions

Unsafe instructions cannot be executed in user mode

#### 2) Memory Isolation

Memory accesses outside a process's address space prohibited

#### 3) Interrupts

Ensure kernel can regain control from running process

#### 4) Safe Transfers

Correctly transfer control from usermode to kernel-mode and back

- What hardware support is necessary to enable protection?
- 61C Review: The Stack?
- How to switch from user mode to kernel mode and back?

#### 1) Privileged Instructions

Unsafe instructions cannot be executed in user mode

#### 2) Memory Isolation

Memory accesses outside a process's address space prohibited

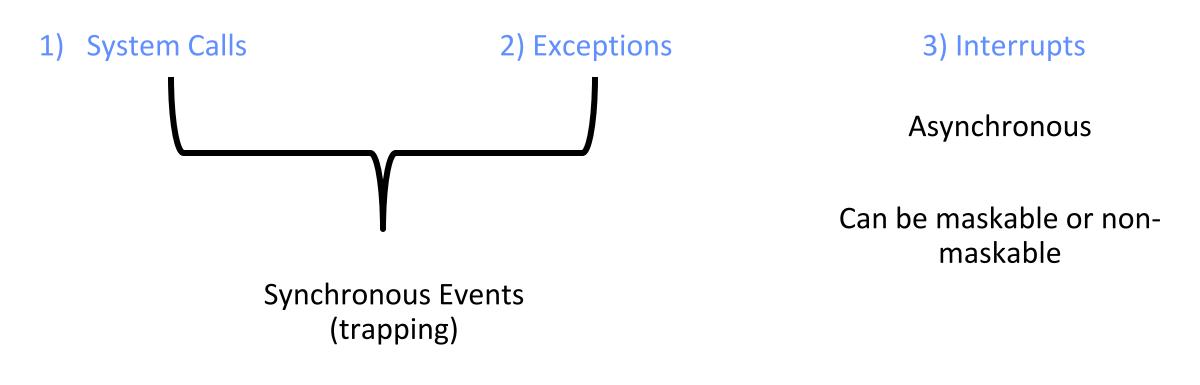
#### 3) Interrupts

Ensure kernel can regain control from running process

#### 4) Safe Transfers

Correctly transfer control from usermode to kernel-mode and back Req 4/4: Safe Control Transfer

# How do safely/correctly transition from executing user process to executing the kernel?



User program requests OS service Transfers to kernel at well-defined location

Synchronous/non-maskable

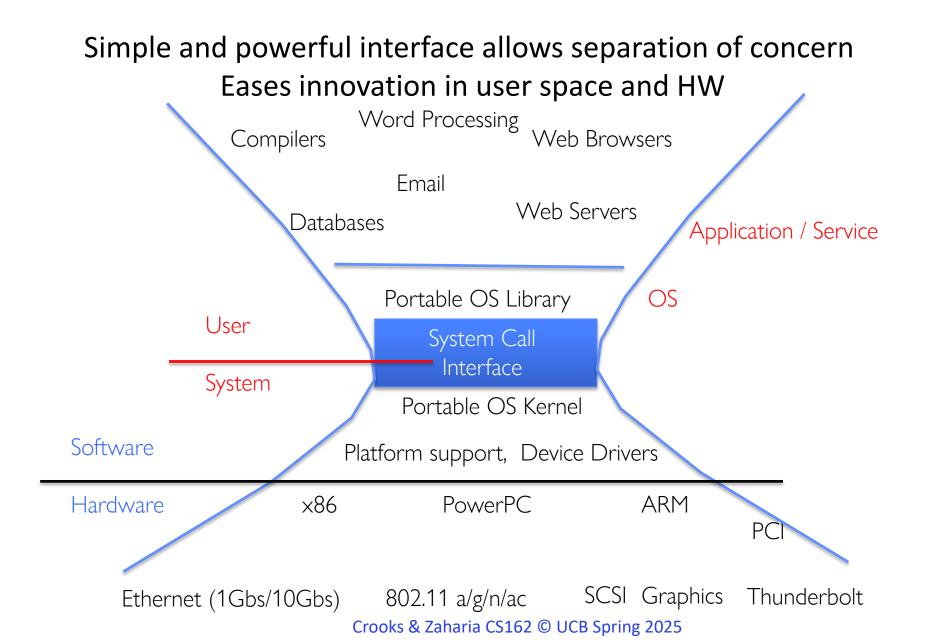
Read input/write to screen, to files, create new processes, send network packets, get time, etc.

How many system calls in Linux 3.0 ? a) 15 b) 336 c) 1021 d) 21121

https://man7.org/linux/man-pages/man2/syscalls.2.html

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## System Calls are the "Narrow Waist"



## System Calls in the Wild (In Linux)

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	13		common		x64_sys_open	
	14			close	x64_sys_close	
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				lstat	x64_sys_new1stat	
	18		common		x64_sys_poll	
				lseek	x64_sys_lseek	

## Safe Control Transfer: Exceptions

Any unexpected condition caused by user program behaviour

Stop executing process and enter kernel at specific exception handler

Synchronous and non-maskable

Process missteps (division by zero, writing read-only memory) Attempts to execute a privileged instruction in user mode Debugger breakpoints!

## Exceptions in the Wild (In Linux)

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	۶۶ master → linux / arch / x8	36 / include	e / asm / trapnr.h	Go to file ····
	joergroedel x86/boot/compre	essed/64: Ad	d stage1 #VC handler	Latest commit 29dcc60 on Sep 7, 2020 🕚 History
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	<pre>1 /* SPDX-License-Identifier 2 #ifndef _ASM_X86_TRAPNR_H</pre>	: GPL-2.0 *	/	
	3 #define _ASM_X86_TRAPNR_H			
	4			
	5 /* Interrupts/Exceptions *	/		
	6	,		
	7 #define X86_TRAP_DE	0	/* Divide-by-zero */	
	8 #define X86_TRAP_DB	1	/* Debug */	
	<pre>9 #define X86_TRAP_NMI</pre>	2	/* Non-maskable Interrupt */	
	10 #define X86_TRAP_BP	3	/* Breakpoint */	
	11 #define X86_TRAP_OF	4	/* Overflow */	
	12 #define X86_TRAP_BR	5	/* Bound Range Exceeded */	
	13 #define X86_TRAP_UD	6	/* Invalid Opcode */	
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	15 #define X86_TRAP_DF	8	/* Double Fault */	
	16 #define X86_TRAP_OLD_MF	9	/* Coprocessor Segment Overrun */	
	17 #define X86_TRAP_TS	10	/* Invalid TSS */	
	18 #define X86_TRAP_NP	11	/* Segment Not Present */	
	19 #define X86_TRAP_SS	12	/* Stack Segment Fault */	
	20 #define X86_TRAP_GP	13	/* General Protection Fault */	
	21 #define X86_TRAP_PF	14	/* Page Fault */	
			And a second	

## Safe Control Transfer: Interrupts

# Asynchronous signal to the processor that some external event has occurred and may require attention

When process interrupt, stop current process and enter kernel at designated interrupt handler

#### Timer Interrupts, IO Interrupts, Interprocessor Interrupts

#### **New Process Creation**

Kernel instantiates datastructures, sets registers, switches to user mode

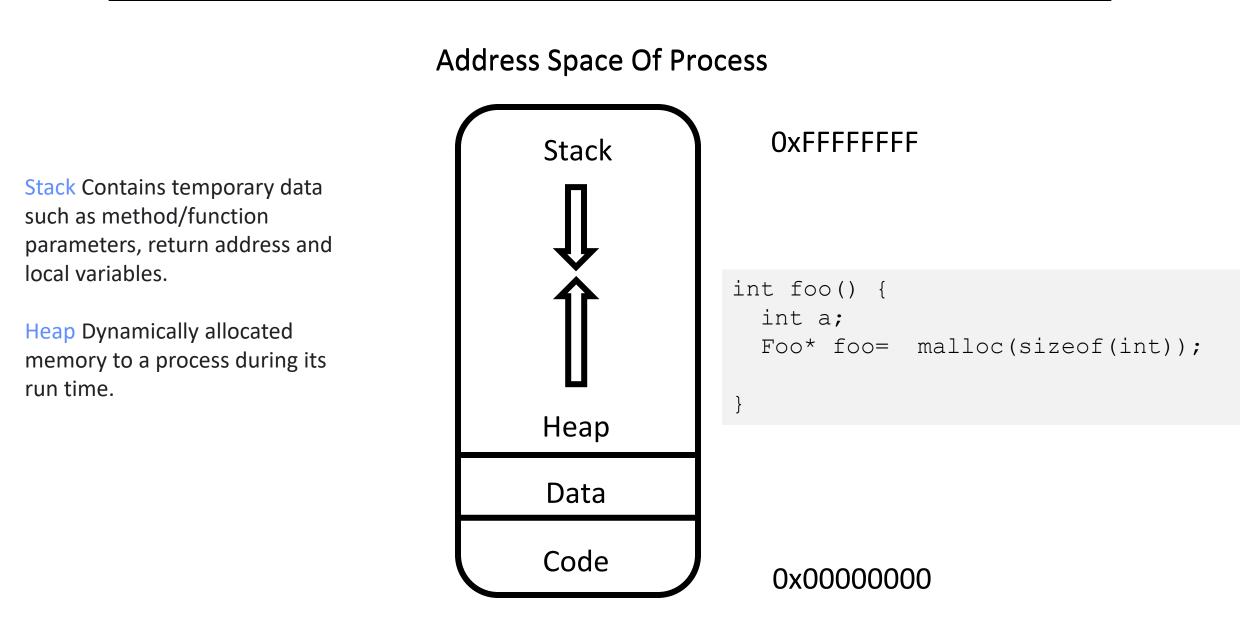
#### Resume after an exception/interrupt/syscall

#### Resume execution by restoring PC, registers, and unsetting mode

#### Switching to a different process

Save old process state. Load new process state (restore PC, registers). Unset mode.

## Goal 2: The Stack is Back (Review)



## Stack Terminology (Review)

#### Stack Frame

#### All the information on the stack pertaining to a function call

Frame Pointer (%ebp)

Contain base address of function's frame.

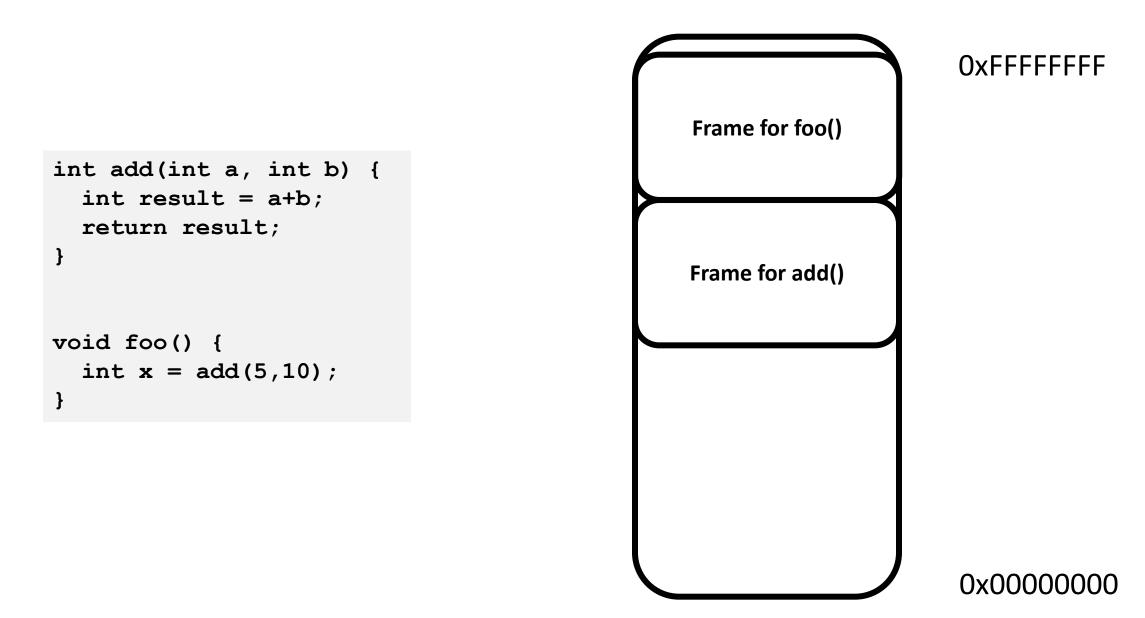
Stack Pointer (%esp)

Points to the next item on the stack.

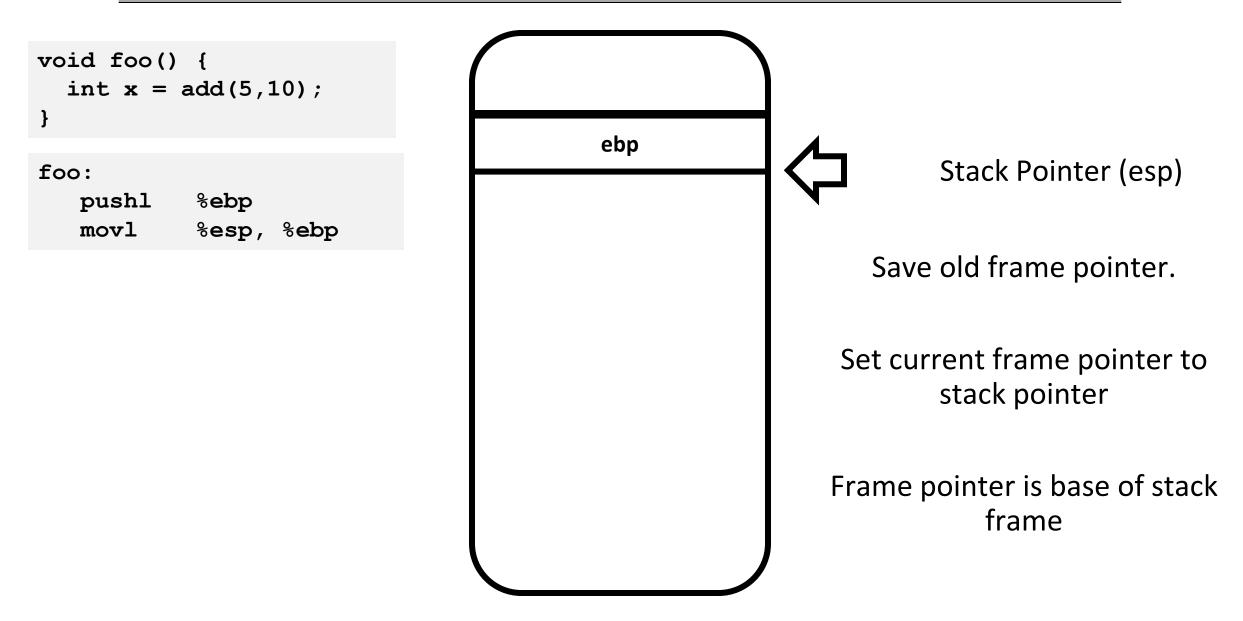
Instruction Pointer (%eip)

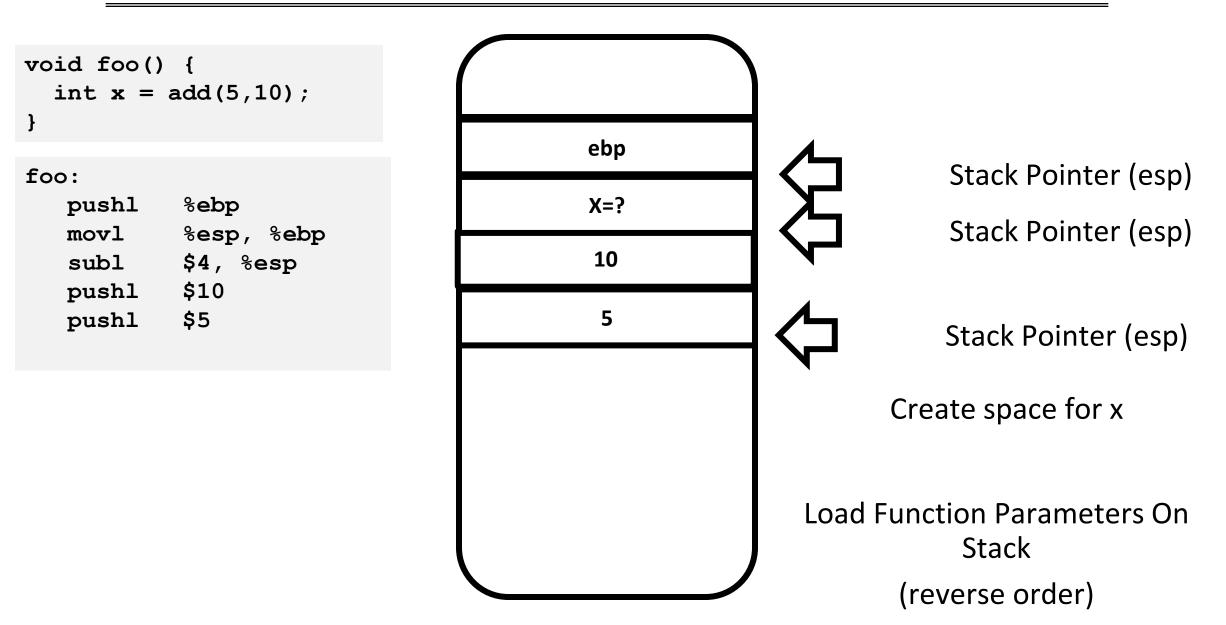
Indicates the current address of the program being executed

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	add:	pushl movl subl	%ebp %esp, %ebp \$4, %esp
<pre>int add(int a, int b) {     int result = a+b;     return result; }</pre>		movl movl addl movl movl leave/r	%eax, -4(%ebp) -4(%ebp), %eax
<pre>void foo() {     int x = add(5,10); }</pre>	foo:	pushl movl pushl pushl	<b>• • •</b>
crooks@laptop> gcc -S -m32 add.c		call movl leave/r	%eax, -4(%ebp)





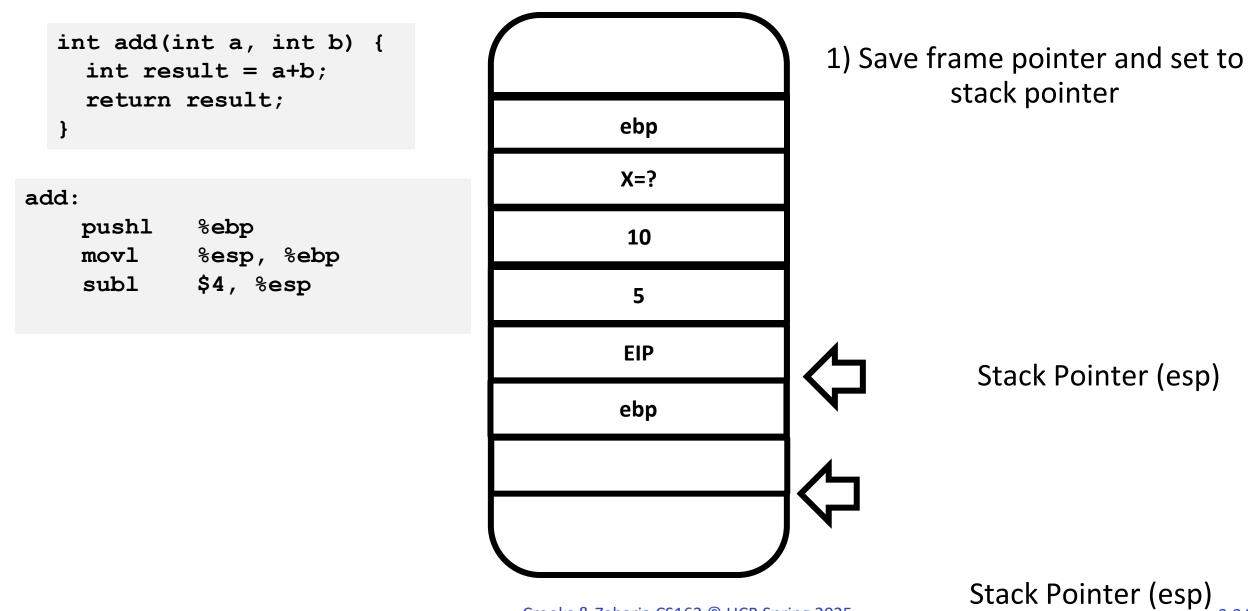
void foo() {
 int x = add(5,10);
}

foo:

pushl	%ebp
movl	%esp, %ebp
subl	\$4, %esp
pushl	\$10
pushl	\$5
call ad	ld

$\bigcap$		
	ebp	
	X=?	
	10	
	5	
	EIP	

Call instruction pushes EIP to stack and jumps to add location



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	at a, int b) { alt = a+b; cesult;	ebp	
add:		X=?	
pushl	%ebp %esp, %ebp	10	12 (%ebp)
subl	\$4, %esp 8(%ebp), %edx	5	8(%ebp)
movl	12(%ebp), %eax %edx, %eax	EIP	
	,	ebp	
			Ctack Deinter (con)
			Stack Pointer (esp)

<pre>int add(int a, int b) {     int result = a+b;     return result; }</pre>	
add: pushl %ebp movl %esp, %ebp subl \$4, %esp movl 8(%ebp), %edx	
<pre>movl 12(%ebp), %eax addl %edx, %eax movl %eax, -4(%ebp)</pre>	

ebp
X=?
10
5
EIP
ebp
result

Local Variables are stored in the stack frame

		<pre>nt a, int b) {     ult = a+b; result;</pre>	
add:			
	pushl	%ebp	
	movl	%esp, %ebp	
	-		
	subl	\$4, %esp	
Ţ	movl	8(%ebp), %edx	
1	movl	12(%ebp), %eax	
	addl	%edx, %eax	
1	movl	%eax, -4(%ebp)	
1	movl	-4(%ebp), %eax	

ebp	
X=?	
10	
5	
EIP	
ebp	
result	

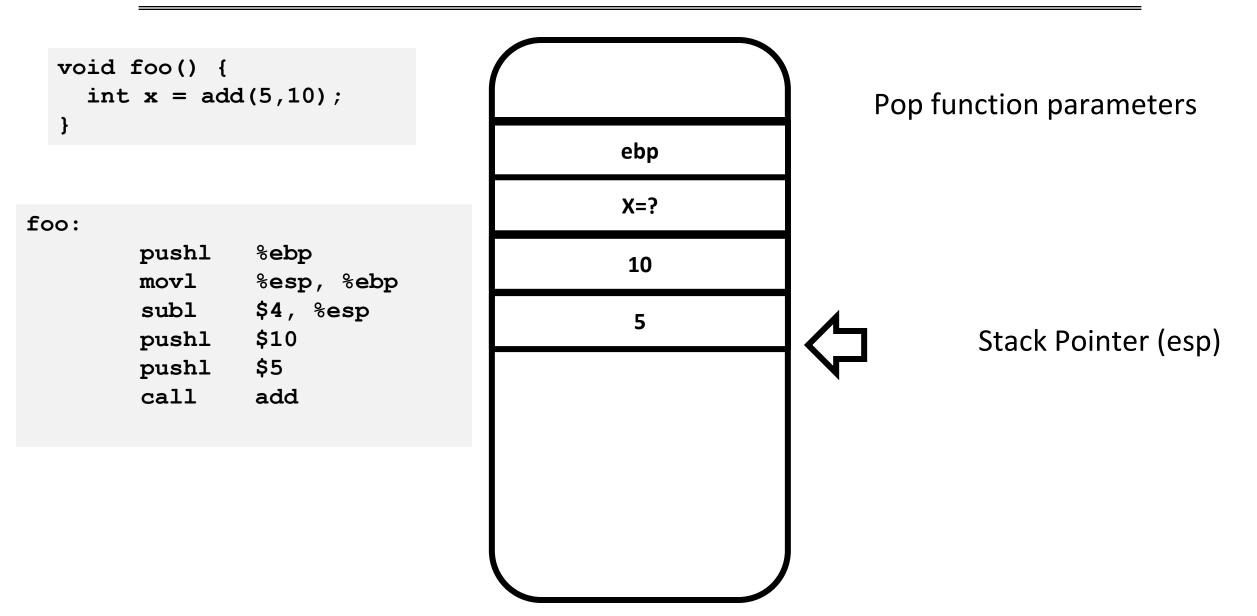
#### Move return value to eax register

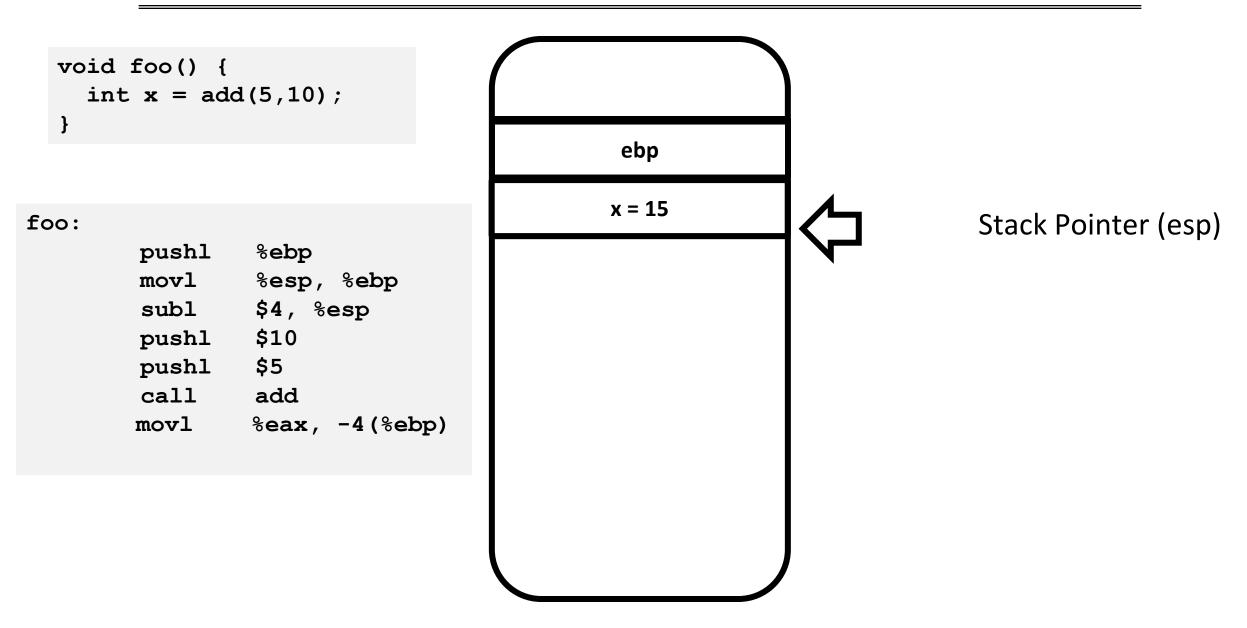
<pre>int add(int a, int b) {     int result = a+b;     return result; }</pre>	
add:	
pushl %ebp	
movl %esp, %ebp	
subl \$4, %esp	
movl 8(%ebp), %edx	
movl 12(%ebp), %eax	
addl %edx, %eax	
movl %eax, -4(%ebp)	
movl -4(%ebp), %eax	
leave	
ret	

ebp
X=?
10
5
EIP
ebp
result

Leave instruction restores caller's frame (pops local variables and ebp)

Return instruction pops EIP and restores control to EIP





# The state of a program's execution is succinctly and completely represented by CPU register state

EIP, ESP, EBP, Eflags/PSW

### Goal 2: User -> Kernel Mode

Key Requirement:

#### Malicious user program (or IO device) cannot corrupt the kernel.

Interrupts, exceptions or system calls handled similarly => fewer code paths, fewer bugs.

#### 1) Limited Entry

Cannot jump to arbitrary code in kernel

#### 2) Atomic Switch

Switch from process stack to kernel stack 3) Transparent Execution

Restore prior state to continue program

## Interrupt Handling Roadmap

#### 1) Processor detects interrupt

- 2) Suspend user program and switch to kernel stack
- 3) Identify interrupt type and invoke appropriate interrupt handler

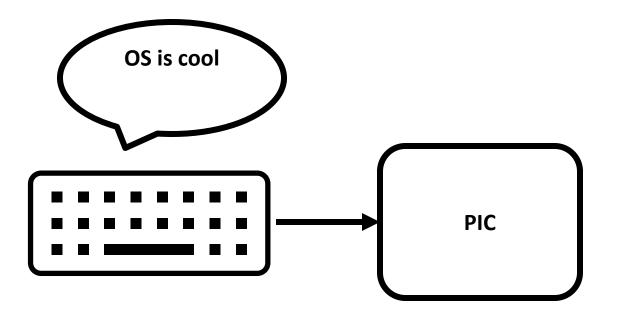
4) Restore user program

## Don't (Hardware) Interrupt Me



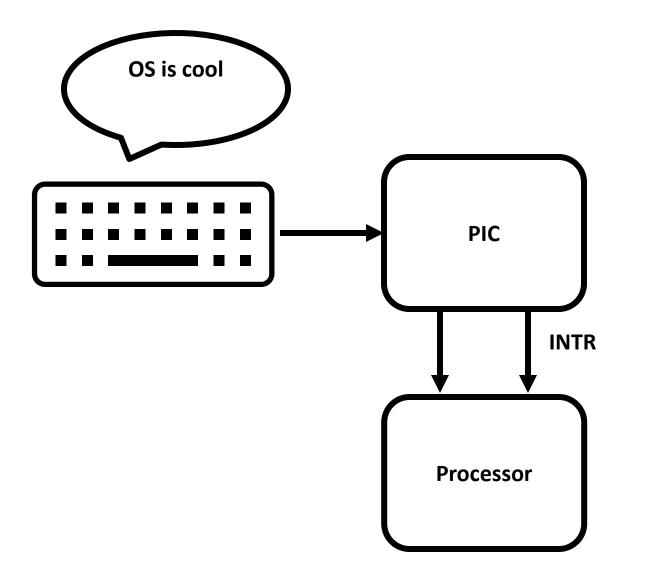
## What happens when I type "OS is cool" on my keyboard while the Add program is running?

## 1) Interrupt Detection (Hardware)



Device sends electric signal interrupt request (IRQ) over interrupt request line to programmable interrupt controller (PIC)

## 1) Interrupt Detection (Hardware)



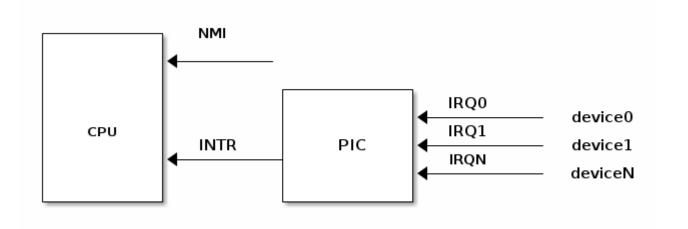
APIC converts IRQ to a vector number and sends signal to processor

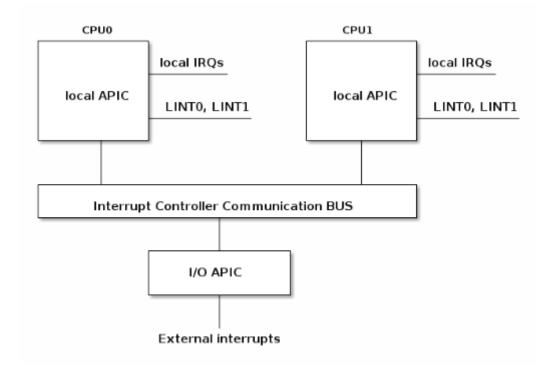
Processor detects interrupt

## IRQs

IRQ	Bus type	Typically used by		
00	none	Non-maskable Interrupt (NMI); system timer		
01	none	Keyboard port		
02	none	Programmable Interrupt Controller (PIC); cascade to IRQ 09		
03	8/16-bit	Communications Port 2 (COM2:)		
04	8/16-bit	Communications Port 1 (COM1:)		
05	8/16-bit	Sound card; printer port (LPT2:)		
06	8/16-bit	Floppy disk controller		

## Sidenote: PICS and APICs





## 2) Save Recovery State (Hardware)

Save register values (recovery state) for process recovery

```
int add(int a, int b) {
    int result = a+b;
    return result;
}
```

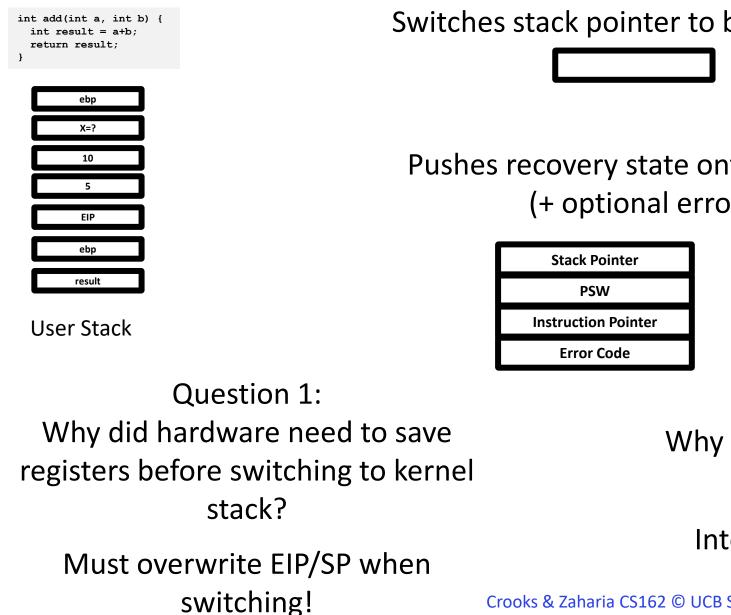
Which registers need to be saved by hardware to restore program?

Stack Pointer (esp)

Program Counter (eip)

Execution Flags / Program Status Word (Eflags)

## 3) Switching (atomically) to Kernel Stack



Switches stack pointer to base of kernel stack

Pushes recovery state onto the new stack (+ optional error code)

> Question 2: Why do we need a separate kernel stack?

Integrity and privacy concerns

## A Tale of Two Stacks

enum procstate { UNUSED, EMBRYO, SLEEPING, RUNNABLE, RUNNING, ZOMBIE };						
// Per-process state						
struct proc {						
uint sz;	// Size of process memory (bytes)					
ode t* padir:	// Page table					
char *kstack;	<pre>// Bottom of kernel stack for this process</pre>					
enum procstate state;	// Process state					
<pre>int pid;</pre>	// Process ID					
<pre>struct proc *parent;</pre>	// Parent process					
struct trapframe *tf:	// Trap frame for current syscall					
<pre>struct context *context;</pre>	// swtch() here to run process					
vold *chan;	// If non-zero, sleeping on chan					
<pre>int killed;</pre>	// If non-zero, have been killed					
<pre>struct file *ofile[NOFILE];</pre>	// Open files					
<pre>struct inode *cwd;</pre>	// Current directory					
<pre>char name[16];</pre>	// Process name (debugging)					
};						

Xv6 Kernel (proc.h) Crooks & Zaharia CS162 © UCB Spring 2025

## 4) Invoke Interrupt Handler (Hardware)

Interrupt vector is an index into Interrupt Vector Table (or interrupt descriptor table).

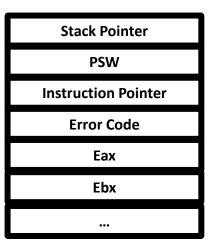
Index contains appropriate Interrupt Handler Routine

Control Unit sets EIP to handler

Handler saves all remaining user registers into stack and implements necessary logic (Transition software)

32	rtc_handler		
33	keyboard_handler		
	floppy_handler		
127	disk_handler		

**IDT Table in Linux** 



**Kernel Stack** 

## 5) Return to Program

# Pop all user registers from kernel stack (restore register state)

Invoke iret instruction to pop saved EIP, EFLAGS, and SP registers from kernel's exception stack to relevant registers

Stack Pointer		
PSW		
Instruction Pointer		
Error Code		
Eax		
Ebx		

Return to user mode

ebp
X=?
10
5
EIP
ebp
result

User Stack

#### **Kernel Stack**

What happens if an interrupt happens while processing an interrupt?

Hardware provides instruction to temporarily defer delivery of interrupt (disable interrupt), and re-enable them when safe (enable interrupt)

Interrupts are disabled when an interrupt handler is running

Periods during which interrupts are disabled should be very short!

## **Interrupt Summary**

1) Device sends signal to APIC

2) Processor detects interrupt

3) Save Recovery State and switch to Kernel Stack

4) Jump to interrupt handler table at appropriate vector. Invoke interrupt handler

5) Restore user program

System calls are user functions that request services from the OS. Described as function call, with a name, parameters and return value.

Good news! Syscalls are handled (almost) identically to interrupts.

## What about syscalls?

32	rtc_handler		
33	keyboard_handler		
	floppy_handler		
127	disk_handler		
128 syscall_handler			

Syscalls issue a "trap" instruction (int 0x80) Generated interrupt will trigger exception vector 128!

How does handler know which syscall to execute? System Call number fed in to %eax register. System call number entry into *system call dispatch table*,

> What about parameters and return values? Propagated through registers.

Warning: Parameters must be carefully checked.

Four differences:

1) Extra-layer of indirection (system call table)

2) Leverage registers for parameters/values

3) When executing iret, increment EIP by one to go to next instruction

4) Usually, interrupts not disabled

## What about exceptions?

### It's the same!

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<> Code 🟦 Pull requests 313 💿 Actions 🖽 Projects 🙂 Security 🗠 Insights					
	۶۶ master ۲ linux / arch / x86 / include / asm / trapnr.h				Go to file ••••
	joergroedel x86/boot/compressed/64: Add stage1 #VC handler				Latest commit 29dcc60 on Sep 7, 2020 🕥 History
	<b>ጸ</b> ኒ 1 c	ontributor			
	32 lines (29 sloc)   1.29 KB				Raw Blame 🖉 💌 🗗 🖞
	1 /* SPDX-License-Identifier: GPL-2.0 */				
	2	<pre>#ifndef _ASM_X86_TRAPNR_H</pre>			
	3 #define _ASM_X86_TRAPNR_H 4				
	5	/* Interrupts/Exceptions */			
	6				
	7	<pre>#define X86_TRAP_DE</pre>	0	/* Divide-by-zero */	
	8	<pre>#define X86_TRAP_DB</pre>	1	/* Debug */	
	9	<pre>#define X86_TRAP_NMI</pre>	2	/* Non-maskable Interrupt */	
	10	<pre>#define X86_TRAP_BP</pre>	3	/* Breakpoint */	
	11	#define X86_TRAP_OF	4	/* Overflow */	
	12	<pre>#define X86_TRAP_BR</pre>	5	/* Bound Range Exceeded */	
	13	<pre>#define X86_TRAP_UD</pre>	6	/* Invalid Opcode */	
	14	<pre>#define X86_TRAP_NM</pre>	7	/* Device Not Available */	
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	16	#define X86_TRAP_OLD_MF	9	/* Coprocessor Segment Overrun */	
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	20	#define X86_TRAP_GP	13	/* General Protection Fault */	
	21	#define X86_TRAP_PF	14	/* Page Fault */	

## The magic of the IVT

Browse the source code of linux/arch/x86/include/asm/irq\_vectors.h

1 /\* SPDX-License-Identifier: GPL-2.0 \*/ #ifndef ASM V86 TPO VECTOPS H

Single, well-defined entry point in the kernel helps with security

#### arch/x86



			#ifndef _ASM_X86_IRQ_VECTORS_H
		3	#define _ASM_X86_IRQ_VECTORS_H
		5	<pre>#include <linux threads.h=""></linux></pre>
36/inc	lude/asm/irq_vectors.h	6	/*
0	0.21 custom trans and exceptions	7	* Linux IRQ vector layout.
0	031, system traps and exceptions	8	*
1		9	* There are 256 IDT entries (per CPU - each entry is 8 bytes) which can
		10	* be defined by Linux. They are used as a jump table by the CPU when a
		11	* given vector is triggered - by a CPU-external, CPU-internal or
		12	* software-triggered event.
		13	*
		14	* Linux sets the kernel code address each entry jumps to early during
32	22, 127, device interrupte	15	* bootup, and never changes them. This is the general layout of the
, z	32127, device interrupts	16	* IDT entries:
		17	*
		18	* Vectors 0 31 : system traps and exceptions - hardcoded events
		19	* Vectors 32 127 : device interrupts
28	int80 syscall interface	20	* Vector 128 : legacy int80 syscall interface
	intoo system interface	21	* Vectors 129 INVALIDATE_TLB_VECTOR_START-1 except 204 : device interrupts
29	129255, other interrupts	22	* Vectors INVALIDATE_TLB_VECTOR_START 255 : special interrupts
		23	*
		24	* 64-bit x86 has per CPU IDT tables, 32-bit has one shared IDT table.
		25	*
		26	* This file enumerates the exact layout of them:
55		27	*/
		28	

Accessing IDT can be slow if not in cache. Syscalls very common, can we make them cheaper?

Allocate a special register (machine specific register) to directly store address of system call dispatch table

Store register call in the rax register

But backwards compatibility ...

• (Continued) Hardware support for dual mode

• 61C Review: The Stack

Privileged Instructions, Memory Isolation, Timer Interrupts, Safe Context Switching.

Stack Pointer, Frame Pointer, Program Counter

• How to switch from user mode to kernel mode and back?

Switch to specified location in kernel & atomic.

Interrupts, Syscalls, Exceptions handled identically. Use of the interrupt vector table